Industry Teaming for Graduate Course Development: A New RFIC Course Sequence at the University of South Florida

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Abstract

Less than ten years ago few people recognized the looming potential for RF/microwave transistors fabricated in silicon due to few mass commercial markets and the RF performance superiority of GaAs at that time. Today silicon radio frequency integrated circuits (RFICs) dominate the wireless landscape and only a small percentage of university programs have faculty with the necessary expertise to teach courses on this leading-edge technology. Henceforth, universities need to become creative to enable instruction of the next generation of engineers to meet these external needs in industry. This paper describes an industry-teaming approach adopted by the University of South Florida to meet this educational challenge.

Introduction

Effective partnering with industry experts can help solve two major constraints in developing advanced, topical course material: a general shortage of educators with relevant experience, and limited funding to support the hiring of new faculty, even if they are available. The Center for Wireless and Microwave Information Systems (the WAMI Center) at The University of South Florida was recently faced with both issues, as its industry advisory board strongly encouraged the development of a graduate course sequence on analog radio frequency integrated circuit (RFIC) design. The solution has been to join forces with local industry experts, serving as adjunct professors, to develop course material in collaboration with WAMI Center faculty.

Now in its second year, the two course sequence covers topics from analog integrated circuit physics to circuit design (e.g. amplifiers and synthesizers) to complete system-on-a-chip radio (Figure 1) development, and culminates in fabrication-ready layouts designed per the IBM SiGe foundry design rules. The breadth of coverage is made possible through contributions of three adjunct professors with extensive industry experience in advanced RFIC design and development.

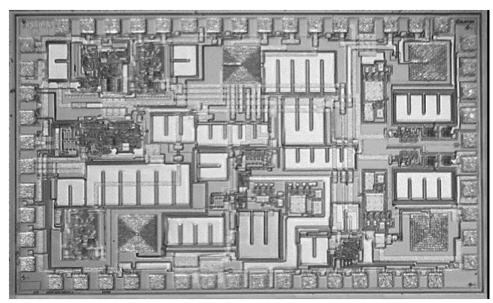

Figure 1 - Complete RFIC on-chip transceiver.

One purpose of this paper is to present the approach that has been taken to transition this mainly adjunct-developed course into the domain of the regular faculty. Other topics that are addressed

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include some challenges presented by the team-teaching approach, a discussion of the student team projects, and the use of industry-type design reviews in the classroom.

Silicon RFIC Background

A primary responsibility of university engineering programs is to produce skilled graduates to meet the needs of industry. In the RF/microwave field, GaAs integrated circuits achieved prominence in the mid-1980's (Figure 2), at roughly the same time that electronic design automation (EDA) tools starting becoming available as 'desk-top' accessories. In the late 80's a small number of schools began to offer GaAs based monolithic microwave integrated circuit (MMIC) courses with extensive EDA use, and the number of course offerings grew into the 1990's. In comparison to the late 90's, however, this was a period of relatively stagnant growth in the *overall* RF/microwave job market and hence skilled faculty could be found to meet these industry needs at the few university programs specializing in this area.

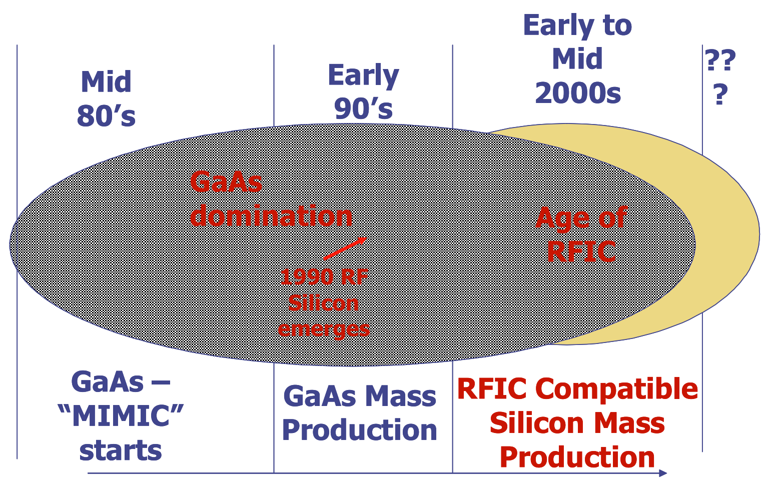

Figure 2 - Evolution of GaAs and silicon RFIC technology.

Now enter the mid-90's, when silicon RF integrated circuits came of age and a simultaneous explosion occurred in the wireless job market. An example of the explosive growth that has occurred in this field over the past decade can be demonstrated by notating the number of publications for SiGe, an important advanced technology and design element in RFIC design. Cressler and Niu performed such a survey in their textbook [1], where they only found 17 publications in 1992 (and 1 three years earlier!), to over 140 refereed articles in 2002. It is estimated today that over 10,000 products have been produced in this short time frame where SiGe devices are utilized in integrated circuit design, leading to a multi-billion dollar industry today. Skilled silicon RFIC designers were scarce and the industry demand was high, leading to the need for relevant university programs and at the same time making it very difficult to recruit the necessary faculty. Today the industry need for young RFIC engineers is beginning to be met at the WAMI Center through a novel educational approach. The industry-teaming approach described in this paper may well be suitable to meet the challenges of the "next" technology revolution.

Course Description

A search for a graduate-level text suitable for a course on silicon RFIC design will likely result in few choices that 'cover all the bases.' The shortage of comprehensive texts is one measure of the newness of the technology. The situation is also indicative of the hybridization of analog IC design and RF circuit design – the very combination that lends so many size, cost and functionality advantages to the RFIC technology.

In order to transition students (who tend to come with microwave course experience) into the RFIC domain the course establishes a firm analog circuit foundation before moving onto the advanced RF aspects. Concepts such as 50 Ohm S-parameters, matching networks and power gain, fundamental to traditional RF/microwave courses, need to be supplemented (and in some cases replaced!) with more conventional analog design techniques. Building from PN-junction, bipolar, and CMOS basic physics, students are taught to think in terms of voltage and current characteristics, and from there to design more complex high frequency transistor circuits utilizing the complete microwave and analog skill set.

The first semester of the two course sequence is based upon the Gray and Meyer text [2] with additional material tailored to modern RF design. Supplemental textbooks for the RF design material are derived from [3] and [4] as well as the adjunct's personal experience. Important advanced Silicon technology discussions revolve around SiGe and RF CMOS. A general listing of the covered topics is given in Table 1. The first semester is fairly traditional in terms of the approach used for assignments, with weekly homework requirements and 4-5 CAD laboratories completed during the semester.

The second semester adopts a case study methodology that mimics the task-oriented IC development process used in industry. A specific technology is chosen as the core topic, e.g. Bluetooth, and supporting lectures provide background material necessary to complete a tapeout ready IC design by semester's end (Table 1). As described below, student teams are formed and each team focuses on a particular part of the IC architecture (amplifier, filter, VCO, etc.) The design is based upon the IBM BiCMOS 5AM 3 level metal process, which has been used extensively in the commercial world for real product over the last 8 years. This process utilizes SiGe transistors with f_Ts of 50GHz, CMOS transistors with Lg minimum = 0.50um, and utilizes a top level thick metal option for inductors with Qs in excess of 30 for certain geometries [publications on SiGe from IBM. Early publications of details for the foundation of this process can be found in [5] and [6].

Team-Teaching Approach

The teaching team is comprised of three adjunct professors from industry and a USF faculty coordinator. The adjunct professors are responsible for generating the majority of the lecture, homework and exam material. The faculty coordinator primarily handles administrative matters such as scheduling, routing of homework and exam material, course web-site maintenance and office hours. Prior to the start of each semester there is considerable interaction among all members of the teaching team on matters such as topic coverage and homework /CAD laboratory assignments, in order to present students with the smoothest progression possible during the semester. During the two-year development cycle, however, the USF faculty are also attending all classes and preparing for the transition of the RFIC course sequence into the normal curriculum (non-adjunct) program. Starting in the third year the adjunct professors will only interact periodically as special guest lecturers – an invitation which will also be extended to a larger pool of practicing engineers.

Utilizing a three-member adjunct team has proven to be advantageous in at least two ways. First, each person has expertise in different, overlapping sub-disciplines of RFIC development, e.g., system-level design, low-noise amplifiers, VCOs, etc. Secondly, the time commitment needed to develop a new, advanced-level two-course sequence is considerable, and the task is virtually impossible for a single, adjunct professor who must contend with work-related design schedules and travel. Lastly, the full time professors can observe the students reactions to different methods of instruction of the material from several different viewpoints, and incorporate the best instructional methods and material in year 3.

Experience has shown that certain aspects of the team-teaching approach can be difficult from the student perspective. Most significantly, each adjunct professor has a unique teaching style – natural variations will occur in areas such as lecture pace and detail, notation, and homework difficulty. For most students it is challenging to "change speed" multiple times during a semester and so, to the extent possible, each adjunct professor is scheduled into consecutive lectures over periods ranging from 3-7 weeks. In addition, it can be challenging to administrate many different instructors with regards to homework collection, grading, and scheduling of lectures in a timely manner conducive to well organized class.

Table 1 - Topics covered in two-semester RFIC course.

Semester I	Semester II
Introduction to RFIC and common receiver architectures	SiGe processes and devices, design fundamentals review
Bipolar devices: p-n junctions, large signal and small signal analysis, heterojunction devices (SiGe)	Electronic design automation tools (Agilent and Cadence), gain and IP3 calculators
MOS devices: large signal and small signal analysis, short channel, weak inversion	IBM SiGe Design Kit introduction and use
Single and multi-stage transistor amplifier architectures	Automatic gain control amplifiers, IQ modulators, voltage/temperature/process variations
Current mirrors and active loads	Electro-static discharge rings, package models
Feedback configurations, operational amplifiers, degenerated configurations	Low noise amplifier, mixer and voltage-controlled oscillator case studies
Noise theory and low noise amplifier design	Bias circuit and baseband filter case studies
Mixers, oscillators and synthesizers	Power amplifier case studies
Power amplifiers, inter-stage matching, multi-stage amplifiers	Interconnect models and layouts

Real-World Features

In order to provide the students access to the best Silicon based RFIC design education possible, it was recognized that access to industry standard CAD tools were essential. Hence, alliances were formed with the leading CAD vendors for students to have access to the most current design tools. The WAMI program has arranged for the use of Cadence and Agilent Silicon IC design tools in the RFDE design environment. This complete suite of tools includes everything that is normally performed in designing a RFIC from schematic capture, design, layout, parasitic extraction and final verifications to create a tapeout ready integrated circuit. In semester 1 and particularly in semester 2, students regularly exercise the software tool base to insure lots of exposure to the RF/analog tools and increase their technical marketability for future employment.

In the second semester of the class sequence the students will collectively design a complete RFIC in an industry tapeout model. This requires the instructors to move from the more traditional educational approach of lecture/exam/homework to a more fluid “hands-on” approach in class. More of this semester is devoted to learning how to create a chip from scratch, rather than the design oriented skills learned in the first semester. The end goal of the second semester is to create a GDSII tapeout quality RFIC for deployment in IBM’s foundry. As a side benefit to the WAMI program, the IC once fabricated can be used for follow-up independent studies and/or development on Masters Thesis and Doctoral Dissertation. The IC can also be used in a larger scope, i.e. wireless system research performed at the university.

The process of creating an RFIC includes the creation of a block level system specification, formation of teams to design the various blocks, and a regimented design review process throughout the semester. The specification was created by the instructors using an existing wireless standard, with low difficulty on the design goals for the individual blocks. This was to insure the designers spent less time on skills that should have been mastered in Semester I and more time on the chip completion activities. In this case, the students were given a Bluetooth compliant specification chosen for its relative low design complexity as compared to cellular, WLAN or other wireless standards. A block diagram of the integrated circuit designed in class is shown in Figure 3.

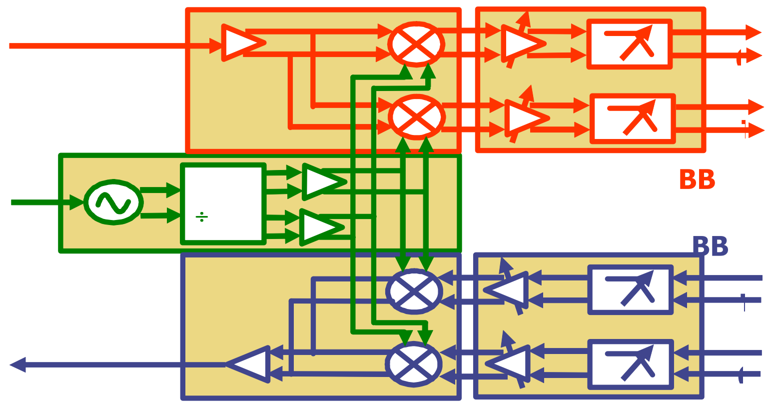

Figure 3 - Block diagram of a typical IC design used in the class.

Five design teams were created of 3-4 students for the following design spaces: RF Receive, RF Transmit, Baseband Receive, Baseband Transmit and Frequency Generation. Students were asked at the beginning of the semester to state their priority of design interest, and from this information the professors organized the students into groups. Teams were very important in the overall scope of the class for the following reasons: first to encourage students to work together on their assignments, second, to help each other over design/software/debugging hurdles and third, to learn to manage different personalities and work ethics that are commonplace in a real-world environment. The design review process was developed to include major design milestones in the process and is shown in Table II.

Table II – Design Review Process

Name	Review	Goals
PCR	Project Concept Review	Circuit Architecture decided, 1st pass design started
PDR	Project Design Review	Design complete, 1st pass layout started
CDR	Critical Design Review	Layout, Statistical analysis, extractions complete
FDR	Final Design Review	All blocks assembled in top level, LVS clean, tapeout

In addition, students were asked to attempt to design to typical variant design environments for an IC. These include variables such as ESD characterization, commercial temperature performance, statistical process variation, power supply rejection, and parasitic extraction of the layout. These are very important elements to designing a tapeout ready IC that are often are overlooked in a university curriculum, yet imperative to producing a commercially viable integrated circuit.

Summary

Effective teamwork has led to the creation of a new graduate-level course sequence on SiGe RFIC technology, helping to support what has quickly become a multi-billion dollar industry in need of skilled designers. The courses have been of widespread interest, attracting prospective students from as far away as Maine through the university's distance education program. Partnering with practicing engineers as adjunct professors has been the key to the success of this effort, as they have contributed not only much needed fundamental expertise but also real-world classroom activities that prepare students for the professional environment that lies ahead. Furthermore, involving multiple adjunct professors (in our case three) has strengthened the developed curriculum and alleviated significant time- and schedule-constraints that are typically unavoidable in these circumstances. Pedagogical issues that arise when students are confronted with multiple teachers in a single semester have been addressed to the extent possible by grouping lectures from each adjunct professor consecutively, and establishing some commonality by including a USF faculty member in all activities. The goal from the outset has been to transition the course responsibilities to full-time USF faculty by the end of the second year.

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Brittin Kane graduated with a Masters of Electrical Engineering at the University of Florida, and a Bachelor of Science in Applied Physics at the University of Maryland BC. He is currently an Engineering Fellow at the Insyte Corporation and Adjunct Professor at University of South Florida. He has over 13 years of experience in Wireless system architecture, RF/analog circuit design, and Silicon based device physics/process integration for RFICs. His chipset applications have included WLAN, Bluetooth, Radiometry, 2G/3G Cellular, as well as Satellite to Satellite communications, utilizing both GaAs and Silicon platforms. He has worked in several prominent semiconductor companies, including Lockheed Martin Research Laboratories, Bell Laboratories – Lucent Technologies, Agere Systems, and RF Solutions (acquired by Anadigics in 2003). Britt also has 7 patents, 6 patent pending applications, and 15 publications in various communications topics such as unique DSP implementations, RF circuit and system design, and CMOS/SiGe technology announcements.

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Mr. Wyatt is an insyte Senior Technical Fellow, providing technical leadership in the core technologies of low power analog and radio frequency integrated circuits (RFIC) and systems. Prior to joining insyte's technical team Mr. Wyatt held the position of Principle Engineering Fellow at Honeywell Space Systems Division. Mr. Wyatt was responsible for helping create an advanced integrated circuits & RF systems design group within Honeywell developing state of the art radio frequency integrated circuits and systems. Mr. Wyatt is an adjunct professor at the University of South Florida helping teach two graduate level RFIC design courses. Mr. Wyatt has greater than 10 US patents in the electronics area and is the inventor of the first fully integrated single-chip L-Band receiver (5,603,111). Mr. Wyatt was the recipient of Honeywell's prestigious H.W. Sweatt Engineer-Scientist Award as well as many other technical awards including EDN's Best Idea of the Year and has published numerous technical papers.